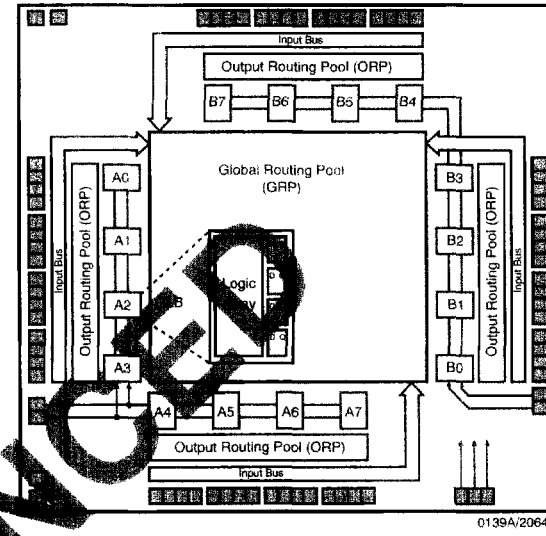
ispLSI® 2064VE

3.3V In-System Programmable SuperFAST™ High Density PLD

Features

- **SuperFAST HIGH DENSITY IN-SYSTEM PROGRAMMABLE LOGIC**
  - — 2000 PLD Gates
  - — 64 and 32 I/O Pin Versions, Four Dedicated Inputs
  - — 64 Registers
  - — High Speed Global Interconnect
  - — Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - — Small Logic Block Size for Random Logic
  - — 100% Functional/JEDEC Upward Compatible with ispLSI 2064V Devices
- **3.3V LOW VOLTAGE 2064 ARCHITECTURE**
  - — Interfaces with Standard 5V TTL Devices
  - — 64 I/O Pin Version is Fuse Map Compatible with 5V ispLSI® 2064 and 2064E
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - — f_{max} = 180 MHz Maximum Operating Frequency
  - — t_{pd} = 5.0 ns Propagation Delay
  - — Electrically Erasable and Reprogrammable
  - — Non-Volatile
  - — 100% Tested at Time of Manufacture
  - — Unused Product Term Shutdown Saves Power
- **IN-SYSTEM PROGRAMMABLE**
  - — 3.3V In-System Programmability (ISP™) Using Boundary Scan Test Access Port (TAP)
  - — Open-Drain Output Option for Flexible Bus Interface Capability, Allowing Easy Implementation of Wired-OR Bus Arbitration Logic
  - — Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality
  - — Reprogram Soldered Devices for Faster Prototyping
- **100% IEEE 1149.1 BOUNDARY SCAN TESTABLE**
- **THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FPGAS**
  - — Enhanced Pin Locking Capability
  - — Three Dedicated Clock Input Pins
  - — Synchronous and Asynchronous Clocks
  - — Programmable Output Slew Rate Control
  - — Flexible Pin Placement
  - — Optimized Global Routing Pool Provides Global Interconnectivity
- **ispEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - — Superior Quality of Results
  - — Tightly Integrated with Leading CAE Vendor Tools
  - — Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™
  - — PC and UNIX Platforms

Functional Block Diagram*



0139A/2064V

Description

The ispLSI 2064VE is a High Density Programmable Logic Device available in 64 and 32 I/O-pin versions. The device contains 64 Registers, four Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2064VE features in-system programmability through the Boundary Scan Test Access Port (TAP) and is 100% IEEE 1149.1 Boundary Scan Testable. The ispLSI 2064VE offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 2064VE device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. B7 (see Figure 1). There are a total of 16 GLBs in the ispLSI 2064VE device. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

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November 1998